Jaeseo Lee

Pohang, South Korea | jaeseolee96@gmail.com | linkedin.com/in/jaeseo-lee-04a96a110

Summary

I specialize in ensuring software reliability and correctness through formal methods and system-level verification. My work focuses on building practical verification frameworks that enhance the safety and robustness of complex software systems. I have developed unified semantic models that integrate program logic with real-world system behaviors, enabling more realistic analysis of embedded and concurrent systems. To ensure scalability in real applications, I design and implement state-space reduction and optimization techniques that improve the efficiency of verification tools. I am particularly interested in applying formal reasoning and automated analysis to strengthen software quality in large-scale, safety-critical systems.

Education

Software Verification Lab. (POSTECH) — *Pohang, South Korea*
MS/Ph.D. in Computer Science and Engineering — *Feb 2017 - Present*

Pohang University of Science and Technology (POSTECH) — *Pohang, South Korea*
BS in Industrial and Management Engineering — *Mar 2011 - Feb 2017*

University of California, Berkeley — *Berkeley, California*
Concurrent Enrollment Program — *Jan 2015 – Dec 2015*

- Coursework: Operating Systems, Architecture, Machine Learning, Compiler, Security

Industry Collaboration Projects

Verification on PLC Programs, with *KSOE (HD Korea Shipbuilding & Offshore Engineering Co., Ltd.)* — *Jan 2020 – Dec 2020*

- Clarified the ambiguous semantics of PLC language described in natural languages
- Devised a bounded linear temporal logic (LTL) model checking method that checks conformity of PLC programs to specifications
- Designed a specification language for expressing desired properties of PLC programs
- Developed STBMC [tool] that integrates the whole process of PLC program verification. This tool generates a counterexample if and only if one exists

Equivalence of LLVM IR Programs, with *GT One* — *June 2017 – Nov 2018*

- Machine-proved semantic equivalence of original and transformed code in security-enhancing transformations
- Developed a lightweight tool with a translation validation approach

Publications

Formal Analysis of Networked PLC Controllers Interacting with Physical Environments — *SAS, 2025*

Jaeseo Lee, Kyungmin Bae [paper]

Formal Semantics and Analysis of Multitask PLC ST Programs with Preemption — *FM, 2024*

Jaeseo Lee, Kyungmin Bae [paper]

Bounded Model Checking of PLC ST Programs using Rewriting Modulo SMT — *FTSCS, 2022*

Jaeseo Lee, Sangki Kim, Kyungmin Bae [paper]

Lightweight Equivalence Checking of Code Transformation for Code Pointer Integrity (in Korean) — *KCSE, 2019.12*

Jaeseo Lee, Tae-Hyoung Choi, Gyuho Lee, Jaegwan Yu, Kyungmin Bae [paper]

Teaching

CSED332: Software Design Methods (TA) *Fall 2017, Fall 2019*

CSED321: Programming Languages (TA) *Spring 2019*

Scholarships

National Science & Technology Scholarship, by KOSAF (Kr. Student Aid Foundation) *Mar 2011 - Feb 2017*

Additional Work Experience

NSW Department of Education *Sydney, Australia*
Jan 2014 - Feb 2014

- Managed and digitized document workflows for efficient record-keeping
- Converted physical records to digital formats and organized signed forms for compliance
- Participated in departmental meetings to observe administrative and policy processes